CLAIMS

We claim:

1. A method comprising:

storing a branch prediction in a queue; and

delivering said stored branch prediction to an instruction fetch unit.

2. The method as in claim 1, comprising generating said branch prediction for two sequential lines in two clock cycles.

3. The method as in claim 1, comprising segmenting a cache of a branch predictor into a first side and a second side, where entries on said first side correspond to addresses having even-numbered indexes, and entries on said second side correspond to addresses having odd-numbered indexes.

4. The method as in claim 3, wherein an index of one of two sequential lines corresponds to an entry on said first side of said cache, and an index of another of said two sequential lines corresponds to an entry on said second side of said cache.

5. The method as in claim 1, comprising, in two cycles, storing said prediction for two sequential lines in said queue and delivering said prediction to said instruction fetch unit.

6. The method as in claim 1, comprising generating branch predictions for a stream of addresses during a stall of said instruction fetch unit.

7. The method as in claim 1, comprising generating during a cycle a prediction for a line, said line being other than the line being fetched by said instruction fetch unit during said cycle.

8. The method as in claim 1, wherein the addresses for which predictions are generated by a branch prediction unit are decoupled from the addresses for which lines are fetched by said instruction fetch unit.

9. A processor comprising:

a branch prediction unit; and

an instruction fetch unit,

wherein said branch prediction unit is to, in a prediction period, generate a prediction on a first line, and said instruction fetch unit is to in said prediction period, fetch instructions for a second line.

10. The processor as in claim 9, wherein said branch prediction unit comprises a queue configured to store branch predictions.

11. The processor as in claim 9, wherein said branch prediction unit is to deliver a branch prediction to said instruction fetch unit in the same prediction period as said branch prediction unit writes said branch prediction to a queue.

12. A processor comprising:

an instruction fetch unit; and

a branch prediction unit, said branch prediction unit comprising a queue to store branch predictions, and said branch prediction unit to deliver branch predictions stored in said queue to said instruction fetch unit.

13. The processor as in claim 12, wherein said branch prediction unit comprises a cache whose entries are segmented into a first side and a second side, where entries on said first side correspond to addresses having even-numbered indexes, and entries on said second side correspond to addresses having odd-numbered indexes.

14. The processor as in claim 12, wherein said cache is to store odd-numbered addresses in a first segment of said cache, and even-numbered addresses in a second segment of said cache.

15. The processor as in claim 12, wherein said branch prediction unit is to look up two lines in a prediction period.

16. The processor as in claim 12, wherein said branch prediction unit is, in a prediction period, to write a branch prediction to said queue and to deliver said branch prediction to said instruction fetch unit.

17. A method comprising:

generating during a cycle, in a branch prediction unit of a processor, a branch prediction for a first line; and

fetching during said cycle, in an instruction fetch unit of said processor, an instruction for a second line.

18. A method as in claim 17, comprising storing said branch prediction in a data storage area of said branch prediction unit.

19. A method as in claim 17, comprising segmenting a cache of said branch prediction unit into a first side and a second side, where entries on said first

side correspond to addresses having even-numbered indexes, and entries on said second side correspond to addresses having odd-numbered indexes.

20. A system comprising:

a dynamic random access memory unit; and

a processor comprising:

an instruction fetch unit; and

a branch prediction unit, said branch prediction unit comprising a queue configured to store branch predictions and said branch prediction unit configured to deliver branch predictions stored in said queue to said instruction fetch unit.

21. A system as in claim 20, wherein said branch prediction unit comprises a cache divided into a first side and a second side, where entries on said first side correspond to addresses having even-numbered indexes, and entries on said second side correspond to addresses having odd-numbered indexes.

22. A system as in claim 21, wherein said cache is configured to store odd addresses in said odd side, and even addresses in said even side.